Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION, APRIL 2018

Course Code: EC207

Course Name: LOGIC CIRCUIT DESIGN (EC, AE)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks

Marks

1 a) Convert the following numbers to the base indicated: (6)

i) $(1542)_8$ to base 10 ii) $52.35)_{10}$ to base 2

iii) $(AD.4)_H$ to base 8 iv) $(1456.125)_{10}$ to base 16

b) Using K map design a 3 bit Binary to Gray code converter. (9)

2 a) Perform the following binary arithmetic using 1's complement and 2's complement. (8)

i) 76.75 - 146.625 ii) 77.5 – 34.25

b) Implement the following Boolean function using 8:1 Multiplexer. (7)

$$F(A,B,C,D) = \bar{A}\bar{B}\bar{C} + B\bar{C}\bar{D} + \bar{A}CD + AC\bar{D}$$

3 a) Design a combinational circuit to compare two 2-bit numbers $A(A_1A_0)$ and $B(B_1B_0)$ and generate outputs $f1 = A > B, f2 = A = B \; and \; f3 = A < B$. (10)

b) How is the Hamming code word generated? The message "1001001" is coded in the 7-bit even parity Hamming code, which is transmitted through a noisy channel. Decode the message, assuming that at most a single error occurred in each code word. (5)

PART B

Answer any two full questions, each carries 15 marks

4 a) Draw the circuit diagram of CMOS NOR gate and explain the working with truth table. (5)

b) Realize the following: (10)

i) T flip-flop using SR flip-flop ii) JK flip-flop using D flip-flop

5 a) Implement the following functions using PLA. (7)

$$F_1 = \sum_m (3,5,7)$$

$$F_2 = \sum_m (4,5,7)$$

b) Realize a T flip-flop using NAND gates and explain the operation with truth table, excitation table and characteristic equation. (5)

c) What is race around condition? How it is avoided? (3)

6 a) Design a MOD-6 synchronous counter using JK flip-flop. When the counter enters an unused state, the counter has to start counting from 0. Draw the timing diagram and complete logic diagram. (10)

b) Define the terms noise margin, propagation delay and power dissipation of logic families. Compare TTL and CMOS logic families showing the values of above mentioned terms. (5)

PART C

Answer any two full questions, each carries 20 marks

7 a) With the logic diagram explain the working of a four bit bi-directional Serial in Serial out (SISO) shift register with mode control. (10)

b) Reduce the following state table using equivalence class state reduction technique. (10)

Present state	Next state and output			
	X=0		X=1	
S0	S0	0	S1	0
S1	S4	0	S2	0
S2	S7	0	S1	0
S3	S2	1	S6	0
S4	S6	0	S5	0
S5	S5	1	S4	1
S6	S1	1	S6	0
S7	S3	0	S8	0
S8	S8	1	S7	1

8 (20)

Obtain the state diagram for a sequence detector to detect the sequence 1010, generate the state table, transition table, excitation table and implement using D flip flop. When the sequence is detected output z = 1, overlapping of sequence is permitted.

9 a) Draw the logic diagram of a 4-bit ring counter and explain the working with timing diagram. (8)

b) Reduce the following state table using implication chart technique. (7)

Present state	Next state and output			
	X=0		X=1	
S0	S4	0	S2	0
S1	S2	0	S0	0
S2	S1	0	S6	0
S3	S6	0	S0	0
S4	S5	1	S1	0
S5	S4	0	S3	0
S6	S3	0	S6	0

c) (5)

Differentiate Moore and Mealy models with examples.

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